REMARKS

Favorable reconsideration and allowance of this application in view of the amendments and remarks to follow are respectfully requested.

The present application contains thirty-one claims, i.e., Claims 1-31, among which Claims 16-31 are withdrawn from consideration and Claims 1-15 are rejected. Applicants have amended Claims 1 and 15 to positively recite that the buried insulating layer has a uniform thickness. Applicants have also amended Claim 1 to further define the location of the SOI layer. Specifically, applicants have added the terms "said SOI layer is located atop said buried insulating layer" into Claim 1. Support for these amendments is found support in paragraphs [0012] and [0018] of the specification, and FIGS. 5 and 7-10 of the specification as well.

Since the above amendments do not introduce any new matter into the present application, entry thereof is respectfully requested.

Claims 1, 2, 6, 9, 10, and 15 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by or, in the alternative, under 35 U.S.C. §103(a) as allegedly obvious over the disclosure of U.S. Patent 6,064,092 to Park, et al. (hereinafter "Park et al."). Further, Claims 3, 7, and 14 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Park et al.

Applicants respectfully submit that Claims 1 and 15, as amended, are not anticipated by the disclosure of Park et al. since the applied reference does not teach the claimed semiconducting devices recited in Claims 1 and 15. That is, Park et al. do not disclose a semiconducting device comprising a channel region located in an SOI layer of an SOI substrate, wherein said channel region is thinned by the presence of *an underlying localized oxide region that is located in said SOI layer* and on top of and in contact with a buried insulating layer of said SOI substrate, *said localized oxide region has outer edges that are aligned with outer edges*

of a gate region that is located above said channel region, said SOI layer is located atop said buried insulating layer, and said buried insulating layer has a uniform thickness.

It is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. *In re King,* 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. *Kloster Speedsteel AB v. Crucible Inc.,* 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that the semiconductor structure disclosed in Park et al. differs from the claimed semiconducting devices in at least four aspects.

First, the buried insulating layer 13 of the present invention has a uniform thickness (see paragraphs [0012] and [0018] and FIGS. 5 and 7-10 of the present application), while the insulating layer 60 of Park et al has an uneven top thereby not having a uniform thickness (see FIGS. 2 and 3D-3F of Park et al.).

Second, in the present invention, the SOI layer 14, in which the thinned channel region 26 is located, is on top of the buried insulating layer 13, while in Park et al., the semiconductor region 40', in which the thinned semiconductor region 73 is located, is embedded in the insulating layer 60. Specifically, as shown in FIGS. 2 and 4-10 of the present application, the bottom surface of the SOI layer 14 is directly on top of the top surface of the buried insulating layer 13. In contrast, the top surface of the insulating layer 60 is uneven, and two portions of the top surface of the insulating layer 60 are at the same horizontal height as the top surface of the semiconductor region 40' of Park et al. (see FIGS. 3E and 3F of Park et al.). In

other words, the semiconductor region 40' of Park et al. is not on top of the insulating layer 60 as the SOI layer 14 of the present application claims to be.

Third, the mesa insulating region 60a of Park et al. is in the insulating layer 60, while the underlying localized oxide region 25 of the present invention is in the SOI layer 14. Specifically, as shown in FIGS. 5 and 7-10 of the present application, there is a distinct interface between the underlying localized oxide region 25 and the buried insulating layer 13. In contrast, the mesa insulating region 60a of Park et al. is merely a flat-topped elevation of the insulating layer 60, and thereby is an integral part of the insulating layer 60. In fact, Park et al. specifically teach that the insulating layer 60 contains the mesa insulating region 60a (see Park et al., column 3, lines 63-66). That is, the mesa insulating region 60a of Park et al. is not in the semiconductor region 40' as the underlying localized oxide region 25 of the present invention claims to be.

Fourth, the localized oxide region 25 of the present invention has outer edges that are aligned with outer edges of the overlying gate region, while Park et al. show that the mesa insulating region 60a has outer edges not aligned with the outer edges of the gate region. Specifically, the outer edges of the mesa insulating region 60a are tapered thereby not having outer edges aligned with the outer edges of the gate region which are vertical (see FIGS. 3E and 3F of Park et al). In contrast, the outer edges of the localized oxide region 25 of the present invention are vertical to the top surface of the buried insulating layer 13 aligning with outer edges of the overlying gate region.

In addition, the plain language of Claims 1 and 15 with respect to the localized oxide region having outer edges that are aligned with outer edges of the overlying gate region describes the pictorial disclosure of FIGS. 5 and 7-10 which illustrate the physical structure of the inventive semiconducting devices. Thus, applicants respectfully submit that the plain

language of Claims 1 and 15 regarding the aligned outer edges of the localized oxide region and the overlying gate region describes a structural feature, not a product-by-process feature.

Therefore, applicants respectfully submit that the semiconductor structure of Park et al. is structurally different from the semiconducting devices of the present invention. Since Claims 2, 6, 9, and 10 are dependent on Claim 1 and include all the limitations thereof, Park et al. do not disclose the subject matter of Claims 2, 6, 9, and 10 either.

In view of the above, Park et al. fail to disclose each and every element of the claims to which it is applied, and thereby the applied reference does not anticipate the present invention. The rejection under 35 U.S.C. §102(b) has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

With respect to the §103(a) rejections, applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness as discussed below.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the cited reference must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the reference, not based on applicants' disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Park et al. neither disclose, nor remotely suggest, a semiconducting device comprising the same physical structure as presently claimed.

Moreover, there is no suggestion available in Park et al. which motivates one skilled in the art to either use an insulating layer having a uniform thickness, as the present invention does, or modify the disclosed mesa insulating region 60a, which is part of the

insulating layer 60, in such a way to arrive at the presently claimed underlying localized oxide region 25, which is in the SOI layer 14. In fact, Park et al. specifically teaches that the mesa insulating region 60a is formed by polishing down the semiconductor substrate 40 to a semiconductor region 40' while the insulating layer 60 is bonded directly to a handling substrate 100 (lines 53 to 67 of column 3, and lines 1-6 of column 4). In view of this disclosed process, the semiconductor-on-insulator substrate of Park et al. would not be able to be obtained by using an insulating layer having a uniform thickness. In other words, an insulating layer having a uniform thickness cannot be used to prepare the semiconductor-on-insulator substrate of Park et al. Furthermore, the disclosed process in Park et al. would not permit formation of the mesa insulating region 60a in the semiconductor region 40'. Unlike Park et al., the underlying localized oxide region 25 of the present invention is formed by conducting an oxygen implantation 40 at a certain implant energy, implant dose, and dummy gate region height thereby forming the localized oxide region 25 in the SOI layer. Therefore, applicants respectfully submit that one skilled in the art, in the absence of specific teaching and in view of the physical structure of the semiconductor-on-insulator substrate of Park et al. and the methods of forming the same, would not be motivated to make a structurally different semiconducting device that is formed through different methods, such as the semiconducting device of the present invention. Applicants further observe that region 60a of Park et al. does not have outer edges that are aligned to outer edges of the gate region.

In view of the above, applicants respectfully submit that Park et al. do not render the present invention obvious. The rejection under 35 U.S.C. §103(a) citing Park et al. has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Claims 4, 5, 8, and 10-13 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over the combined disclosures of Park et al. and U.S. Patent No. 6,479,866 to

Xiang (hereinafter "Xiang"). Claim 6 stands rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Park et al. further in view of the admitted prior art. More specifically, the Examiner alleges that Xiang teaches that the damaged region 90 can be formed separately from the buried insulating layer 20.

Applicants respectfully submit that the present invention is not rendered obvious by the combined disclosures of Park et al. and Xiang because the cited references, solely or in combination, do not teach, recognize, or suggest the claimed semiconducting device.

As discussed previously, Park et al. do not disclose or suggest a semiconducting device comprising the same physical structure of the semiconducting device of the present invention. Moreover, region 60a of Park et al. does not have outer edges that are aligned to outer edges of the gate region. Xiang discloses a semiconductor device that includes a transistor on an SOI wafer having a subsurface recombination area at least partially within its body. However, the semiconductor device of Xiang is different from the claimed semiconducting devices in at least two aspects. First, the buried insulating layer 13 of the present invention has a uniform thickness (see paragraphs [0012] and [0018] and FIGS. 5 and 7-10 of the specification), while the buried insulator layer 20 of Xiang has an uneven top thereby not having a uniform thickness (see FIGS. 1 and 3-10 in Xiang). Second, the localized oxide region 25 of the present invention has outer edges that are aligned with outer edges of the overlying gate region, while Xiang shows that the damaged region 90 has outer edges <u>not</u> aligned with the outer edges of the gate region in FIGS. 1, 9, and 10. Therefore, the cited references, solely or in combination, fail to disclose or suggest a semiconducting device comprising a channel region located in an SOI layer of an SOI substrate, wherein said channel region is thinned by the presence of an underlying localized oxide region that is located in said SOI layer and on top of and in contact with a buried insulating layer of said SOI substrate, *said localized oxide region has outer edges that are aligned with*

outer edges of a gate region that is located above said channel region, said SOI layer is located atop said buried insulating layer, *and said buried insulating layer has a uniform thickness*.

The §103(a) objections also fail because there is no suggestion available in the cited references which motivates one skilled in the art to modify the disclosed devices in such a way to arrive at the device of the present invention.

As discussed previously, Park et al. fail to provide any suggestion which motivates one skilled in the art to either use a buried insulating layer having a uniform thickness or form the mesa region 60a in the SOI layer. Park et al. also do not teach or suggest a structure in which region 60a has outer edges that are aligned to outer edges of an overlying gate region. Xiang discloses a semiconductor-on-silicon device having reduced floating body effects. More specifically, Xiang intends to resolve the problem of undesirable floating body effects in field effect transistors (column 3, line 62 to column 4, line 10), and provides a transistor having one or more damaged recombination regions within the body of the transistor. In contrast, the present invention intends to resolve the problem of high external resistance in ultra-thin channel SOI devices, and provides a thin SOI device having low external resistance without raised source/drain regions. Notably, Xiang does not in any manner comment on the problem of high external resistance in ultra-thin channel SOI devices. With regard to the damaged region 90, Xiang specifically teaches that the presence of the damaged region 90 within the body 38 greatly increases the recombination rate within the body, thus reduces the tendency of the body to build up a floating body potential (column 4, lines 3-10). Xiang also teaches the location and size of the damaged region 90. However, Xiang does not suggest applying the damaged region 90 to a semiconducting device of Park et al. in such a way to form the mesa region 60a of Park et al. in the SOI layer. Thus, there is no motivation provided in the applied references, or otherwise of record, to modify the disclosed semiconductor-on-insulator substrates to include applicants'

claimed semiconducting device. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Vaeck*, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

In addition, none of the admitted prior art cures the deficiency of Park et al. Therefore, applicants respectfully submit that the present invention is not rendered obvious by Park et al. further in view of the admitted prior art.

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remark, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Leslie S. Szivos, Ph.D.
Registration No. 39,394

Scully, Scott, Murphy & Presser, P.C.
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343

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